FEATURES

MitySOM-5CSX Development Board

MitySOM-5CSX SoM Module

Additional Hardware Included:

- UART to USB Cable
- Ethernet Cable
- AC to DC 24V 2.7A Adapter

Integrated +2.5V/+3.3V/+5V/+12V Power Supplies

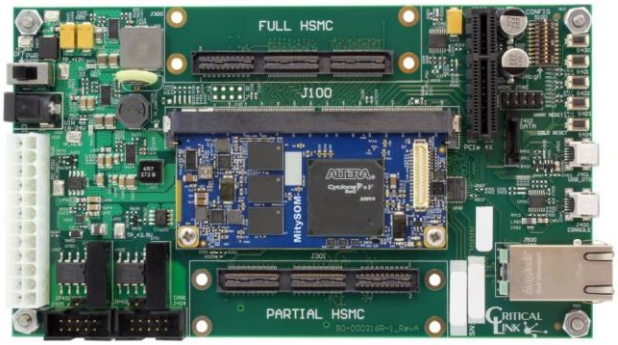
ATX Power Supply Compatible

Digital Interfaces:

- 10/100/1000 MBit Ethernet Interface
- Debug UART to USB
- USB OTG Interface
- Dual Electrically Isolated CAN Bus Interfaces
- SD/MMC Card Socket

Expansion

- Full HSMC Interface
- Partial HSMC Interface
- PCI-e x4



Software and Documentation:

- Linux Kernel
- uBoot
- Development Environment - Virtual Machine
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

APPLICATIONS

- MitySOM-5CSX Evaluation
- Test and Measurement
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Test and Measurement
- Rapid Prototyping

DESCRIPTION

The MitySOM-5CSX Development Kit provides all the hardware and software support for system designers and developers to evaluate the Critical Link MitySOM-5CSX System on Module. The MitySOM-5CSX Development Kit comes complete with the MitySOM-5CSX module that meets your project's needs.

The MitySOM-5CSX Development Kit includes on-board Debug UART to USB converter, 10/100/1000 GBit Ethernet, Universal Serial Bus (USB 2.0) USB-On-The-Go (OTG) communication interfaces. Full and Partial HSMC connectors are compatible with a wide range of existing add-on cards, dual electrically isolated CAN and PCI-e x4 expansion ports provide a comprehensive set of interface options.

Multi Media Card (MMC) interface supporting Secure Digital (SD) cards. Configuration dip-switches, debug switches, RTC battery and a SOM current input monitoring circuit round out the Development Kit. All powered from a single 24VDC input (adapter included) or a standard ATX PC power supply with onboard +2.5V/+3.3V/+5V/12V power supplies.

A block diagram of the MitySOM-5CSX Development Kit is illustrated in Figure 1 on the following page. Control of the on-board interface hardware and connected Expansion IO cards require proper configuration of the MitySOM-5CSX Module. While not required, it is strongly recommended that the MitySOM software development kit and supplied API be used to manage these interfaces.

MitySOM-5CSX Development Kit

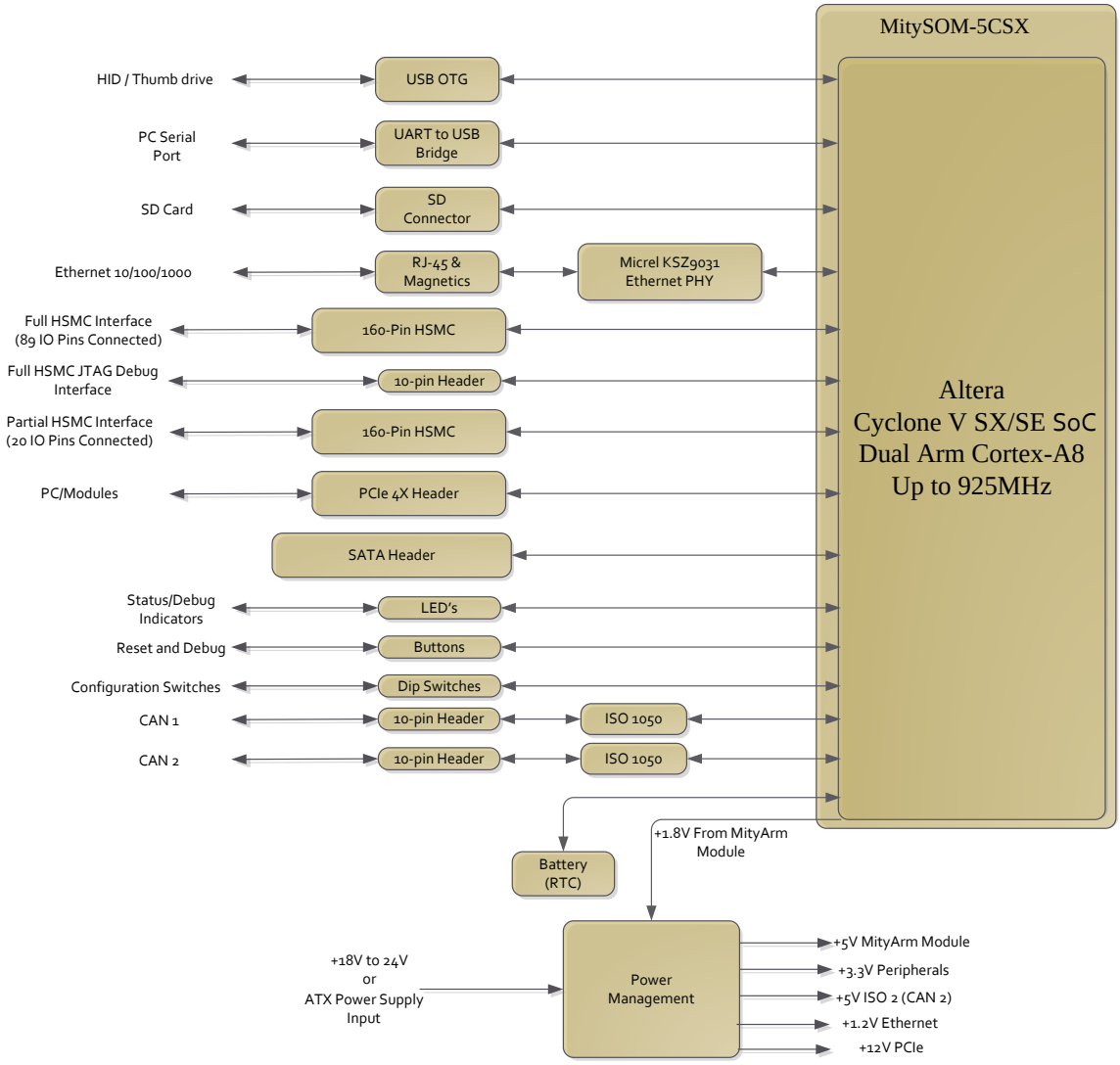


Figure 1: MitySOM-5CSX Development Kit Block Diagram

Additional details about the Cyclone V SX/SE SoC, available peripherals, their features and FPGA IO details are provided in the data sheet at the Altera website (http://www.altera.com/devices/processor/soc-fpga/cyclone-v-soc/cyclone-v-soc.html).

Feature Descriptions

Electrical Interface Descriptions

Debug UART to USB Interface Description

The on-board UART to USB Bridge, FTDI FT230X, provides a serial interface at data rates up to 115,200 baud. The USB serial interface, J400 - Console, is routed to the primary MitySOM serial bootloading port, UART0. It allows for general module debug, remote code download and FLASH upgrades on an attached MitySOM from this connector when interfaced with a PC.

When connected to a Windows XP, Vista, 7 or 8 PC no drivers are required as Windows Update is used to obtain the drivers.

USB 2.0 Interface Description

The on-board USB OTG interface utilizes a mini B type connector J401 and interfaces with the USB phy on the MitySOM-5CSX module. This phy is connected to the USB0 controller within the Cyclone V SoC HPS. Linux drivers are available. This interface allows for a connection to either a PC or a USB device through the use of a USB-OTG to USB A type adapter, not included.

MultiMedia Card (SD) Interface Description

The on-board MultiMedia Card (MMC) slot uses a Secure Digital connector J403 which supports standard (3.3V) cards. U-Boot configuration information and Linux drivers are available.

Gigabit Ethernet Interface Description

The on-board Ethernet interface features a Micrel KSZ9031 Ethernet PHY capable of running at 10/100/1000Mbit including link auto-negotiation and RGMII/MDIO capability. An industry standard RJ-45 connector is provided for external connection. This Ethernet interface may be used to perform remote code download via U-Boot and FLASH upgrades on an attached MitySOM-5CSX module in addition to standard network interfacing.

SATA Interface Description

The on-board SATA connector allows for connection to the MitySOM-5CSX module gigabit transceivers. To take advantage of the SATA interface an IP core needs to be used. There are a number of companies that offer such cores and you can contact your Critical Link representative for a recommendation.

RTC Battery (VBat)

The MitySOM-5CSX Development Board includes a battery retainer which is identifier BH600. This retainer houses the Panasonic CR-1025/BN which is used to power the RTC on the module. The battery switch, which is located next to the retainer, connects or isolates the battery ground and the board ground switching the RTC supply on or off. Note that if the battery gets discharged, below 1.2V, a new battery may be required for proper module function. If the battery voltage is between 1.2V and 1.8V a slower JTAG clock frequency may be needed for JTAG debugging. Please contact a Critical Link representative for details.

Full HSMC Interface Description

The Full High Speed Mezzanine Card (HSMC) interface allows for the use of add-on cards that are designed for the Altera Cyclone V on the MitySOM-5CSX module. A number of "off the shelf" boards/kits are available from Critical Link and other third parties that are compatible with this interface.

Full HSMC JTAG Debug Interface Description

The 10-pin JTAG header J302 is available onboard for debugging of a device that is connected to the Full HSMC connector, J300.

Partial HSMC Interface Description

The Full High Speed Mezzanine Card (HSMC) interface allows for the use of add-on cards that are designed for the Altera Cyclone V on the MitySOM-5CSX module. This interface offers access to a single Gigabit transceiver interface as well.

PCI-e x4 Interface Description

The on-board 4-channel PCI-e interface provides both root port and endpoint mode support for PCI-e x1, x2 and x4 devices when a MitySOM-5CSX is used. In addition an on-board 100MHz clock is provided as well as +12V and +3.3V external power supplies.

Dual CAN Interface Description

The on-board CAN provides a set of CAN V2.0B compliant interfaces. These interfaces are managed by the MitySOM-5CSX module directly.

The galvanic isolation is provided by a dedicated TI ISO1050 transceiver for each interface. The ISO1050 is powered by an isolated power supply with 1000V* isolation from the primary supply.

Jumpers JP400 (CAN 1) and JP401 (CAN 0) can provide dedicated bus termination of 120Ohm. To enable termination, place shorting jumper across JP504.

The electrical interfaces are provided via J404 (CAN1) and J405 (CAN0), 10-pin shrouded headers.

Linux Driver and API examples are available to support CAN functionality.

Debug/User Switch Descriptions

A total of 5 switches are present on the 5CSX Development Kit.

S400, S401 and S402 are tied to HPS GPIO pins on the module edge connector; pins 252, 264 and 266 respectively. These switches can be utilized for any user defined functions.

S403 is for the HPS Warm Reset which just causes the MitySOM Cyclone V SoC to perform a soft reset.

S404 is for the Cold Reset which causes the MitySOM input power supply to be toggled.

Boot Configuration Dip-Switch Description

The 5CSX Development Kit features a series of 10 clock and boot configuration dip-switches. These dip switches determine the order of peripherals for a valid boot image as well as the clock source selection.

MSEL (5 Switches), CLKSEL (2 Switches) and BOOTSEL (3 Switches) are configured via S100.

By default the MitySOM-5CSX Development Kits is required to boot initially from the MMC/SD card.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	25.2 V
Storage Temperature Range	0 to 80C

OPERATING CONDITIONS

Ambient Temperature Range	-40 to 85C*
Humidity	0 to 95% Non-condensing

* Ambient Temperature Range excludes components in the table below:

CLPN	Quantity	Designator	Description	Min Temp (C)	Max Temp (C)	Manufacturer	Manufacturer PN
12728	1	S600	SWITCH SLIDE SPDT 5A 120V	-30	85	E-Switch	500SSP1S2M2QEA
6579	5	S400, 401, 402, 403, 404	SWITCH TACTILE SPST-NO 0.05A 12V	-30	85	Panasonic	EVQ-PE105K
8861	1	NA	BATTERY LITHIUM 3V COIN 10MM	-30	60	Panasonic	CR-1025/BN

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Maximum Power Supply Output					
I_{Max}	24V Supply (AC Adapter) all components			2.7	A
I_{Max}	12.0V Supply[1] for external components			2.0	A
I_{Max}	5.0V Supply[1] for external components			2.0	A
I_{Max}	3.3V Supply[1] for external components			3.0	A
Power Dissipation					
V_S	Supply Voltage		24±5%		V
I_S	Supply Current[2]		250		mA

Notes:

1. The maximum current supplied to external components should be limited to the specified maximum for all externally connected power supplies
2. PCI-e/HSMC cards not attached, 100% ARM utilization, RS-232 and Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – J601 and J600

The MitySOM-5CSX Development Kit power interface, J601, requires a single +24Volt power supply. A recommended input supply rating of at least 2A is recommended and a 2.7A supply is included with each Development Kit.

Table 1: Input Power Interface Pin Description

Signal	J601 Position
+24V	1
GND	2

Additionally the MitySOM-5CSX Development Kit provides a standard ATX PC power supply connector, J600, which can be utilized; power supply not included. Any supply capable of 100W or more is recommended. When this type of input supply is used J601 should NOT be connected.

Note that when an ATX power supply is used there is no control logic on the Development Kit so when connected the Development Kit will be powered unless an external switch is used or the supply is unplugged from AC power.

Main Power Switch – S600

An input power switch is present on the Development Kit, S600, which controls the power input, on or off, from J601. It has no effect on the ATX power supply input, J600.

MultiMedia Card (SD) Interface – J403

The MitySOM-5CSXx Development Kit provides a MMC interface that uses a standard Secure Digital (SD) card slot for the physical interface. Through the use of SD card adapters MicroSD and MiniSD cards can be used in this slot. By default the slot is supplied with 3.3V for use with standard SD cards and the R140 resistor can be de-populated while R139 is populated to provide a 1.8V supply for SDHC cards.

Debug/Boot UART - USB Interface – J400

Table 2: J400 Mini USB Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VBUS	Power	-	
2	D-	I/O	USB 2.0	USB data minus line
3	D+	I/O	USB 2.0	USB data plus line
4	GND	GND	-	
5	SHIELD	GND	-	

USB 2.0 Interface (OTG) – J401

Table 3: J401 Pin Assignments

Pin	Signal	Type	Standard	Notes
1	USB1_VBUS	POWER	-	
2	USB1_D_N	I/O	USB 2.0	USB data minus line
3	USB1_D_P	I/O	USB 2.0	USB data plus line
4	USB1_ID	I/O	-	
5	GND	POWER	-	

Dual CAN Interface – J404 & J405

Table 4: J404 CAN1 & J405 CAN0 Connector[1] Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RESERVED	-	-	
2	CANL	I/O		CAN Bus Signal L
3	GND_ISOCANx[2]	Power	-	CAN Bus Isolated Ground
4	RESERVED	-	-	
5	RESERVED	-	-	
6	RESERVED	-	-	
7	CANH	I/O		CAN Bus Signal H
8	RESERVED	-	-	
9	+5V_CANx[2]	Power	-	Isolated +5V Output, 20mA Max
10	RESERVED	-	-	

Note 1: Please see Figure 2 for physical pin-out of connector
Note 2: The 'x' at the end of the signal names is either a 1 or a 0 depending on which CAN interface you are using.

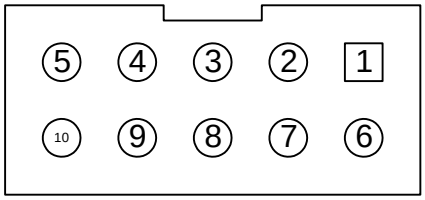


Figure 2: J404 and J405 Pin-out (Top View)

SATA Interface – J402

Table 5 describes the pin-out of the SATA connector on the MitySOM-5CSX development board. A SATA core is needed in the FPGA fabric to utilize this interface.

Table 5: J402 Pin Assignments

Pin	Signal	SoM Pin	Type	Standard	Notes
1	GND	-	POWER	-	
2	SATA_RX_C_P	232	I	-	
3	SATA_RX_C_N	234	I	-	
4	GND	-	POWER	-	
5	SATA_TX_C_N	241	O	-	
6	SATA_TX_C_P	239	O	-	
7	GND	-	POWER	-	

PCIe Interface – J200

Table 6 describes the pin-out of the PCI-e x4 capable interface on the MitySOM-5CSX development board. The I/O "type" is in reference to the signal direction from the SoM/development board.

Table 6: J200 Pin Assignments

Pin	Signal	SoM Pin	Type	Standard	Notes
A1	GND	-	POWER	-	
A2	+12V_EXT	-	POWER	1A Max	Note 2
A3	+12V_EXT	-	POWER	1A Max	Note 2
A4	GND	-	POWER	-	
A5	JTAG2	-	-	-	TCK – 2.2k ohm resistor to ground
A6	JTAG3	-	NC	-	TDI – No connect
A7	JTAG4	-	NC	-	TDO – No connect
A8	JTAG5	-	NC	-	TMS – No connect
A9	+3.3V_EXT	-	POWER	1A Max	Note 1
A10	+3.3V_EXT	-	POWER	1A Max	Note 1
A11	PCIE1_PERST_SJN	21	I	-	
A12	GND	-	POWER	-	
A13	PCIE_CLK0_R_P	-	O	-	100MHz clock, U200, to PCI-e device
A14	PCIE_CLK0_R_N	-	O	-	100MHz clock, U200, to PCI-e device
A15	GND	-	POWER	-	
A16	PCIE1_RX_0_P	204	I	-	
A17	PCIE1_RX_0_N	202	I	-	
A18	GND	-	POWER	-	
A19	RESERVED	-	-	-	
A20	GND	-	POWER	-	
A21	PCIE1_RX_1_P	208	I	-	
A22	PCIE1_RX_1_N	210	I	-	
A23	GND	-	POWER	-	
A24	GND	-	POWER	-	
A25	PCIE1_RX_2_P	214	I	-	
A26	PCIE1_RX_2_N	216	I	-	
A27	GND	-	POWER	-	
A28	GND	-	POWER	-	
A29	PCIE1_RX_3_P	226	I	-	
A30	PCIE1_RX_3_N	228	I	-	
A31	GND	-	POWER	-	
A32	RESERVED	-	-	-	
B1	+12V_EXT	-	POWER	-	
B2	+12V_EXT	-	POWER	-	
B3	+12V_EXT	-	POWER	-	
B4	GND	-	POWER	-	
B5	PCIE1_SMCLK	69	I	-	
B6	PCIE1_SMDAT	71	I/O	-	
B7	GND	-	POWER	-	
B8	+3.3V_EXT	-	POWER	1A Max	Note 1
B9	JTAG1	-	NC	-	TRSTn – No connect
B10	+3.3V_EXT	-	POWER	1A Max	Note 1
B11	PCIE1_WAKEN	83	O	-	
B12	RESERVED	-	-	-	
B13	GND	-	POWER	-	
B14	PCIE_TX_0_P	209	O	-	
B15	PCIE_TX_0_N	211	O	-	
B16	GND	-	POWER	-	
B17	PCIE1_X1_PRSNT2N	101	I	-	

B18	GND	-	POWER	-	
B19	PCIE_TX_1_P	215	O	-	
B20	PCIE_TX_1_N	217	O	-	
B21	GND	-	POWER	-	
B22	GND	-	POWER	-	
B23	PCIE_TX_2_P	221	O	-	
B24	PCIE_TX_2_N	223	O	-	
B25	GND	-	POWER	-	
B26	GND	-	POWER	-	
B27	PCIE_TX_3_P	233	O	-	
B28	PCIE_TX_3_N	235	O	-	
B29	GND	-	POWER	-	
B30	RESERVED	-	-	-	
B31	PCIE1_X4_PRSNT2N	162	I	-	
B32	GND	-	POWER	-	

Notes:
1. The maximum total current supplied to external components from the +3.3V supply should be limited to less than 3.0A. The maximum current allowed per connector pin is 1A.
2. The maximum total current supplied to external components from the +12V supply should be limited to less than 2.0A. The maximum current allowed per connector pin is 1A.

Full HSMC Interface- J300

Table 7 describes the pin-out of the Full HSMC interface on the MitySOM-5CSX development board. The I/O "type" is in reference to the signal direction from the SoM/development board.

Table 7: J300 Connector Pin Assignments

Pin	Schematic Signal	SoM Pin	Type	Standard	Notes
1 - 32	RESERVED	-	-		
33	HSMC1_SMSDA	54	I/O	2.5V	Bank 4A
34	HSMC1_SMSCL	56	O	2.5V	Bank 4A
35	HSMC1_JTAG_TCK	-	-		J302 – Pin 1
36	HSMC1_JTAG_TMS	-	-		J302 – Pin 5
37	HSMC1_JTAG_TDO	-	-		J302 – Pin 3
38	HSMC1_JTAG_TDI	-	-		J302 – Pin 9
39	HSMC1_CLKOUT0	160	O	2.5V	Bank 3B
40	HSMC1_CLKIN0	99	I	2.5V	Bank 3B
41	HSMC1_D0	74	I/O	2.5V	Bank 4A
42	HSMC1_D1	90	I/O	2.5V	Bank 4A
43	HSMC1_D2	76	I/O	2.5V	Bank 4A
44	HSMC1_D3	106	I/O	2.5V	Bank 4A
45	+3.3V	-	Power	1A Max	Note 1
46	+12V	-	Power	1A Max	Note 2
47	HSMC1_TX0_P	68	I/O	2.5V	Bank 4A
48	HSMC1_RX0_P	87	I/O	2.5V	Bank 4A
49	HSMC1_TX0_N	70	I/O	2.5V	Bank 4A
50	HSMC1_RX0_N	89	I/O	2.5V	Bank 4A
51	+3.3V	-	Power	1A Max	Note 1
52	+12V	-	Power	1A Max	Note 2
53	HSMC1_TX1_P	78	I/O	2.5V	Bank 4A
54	HSMC1_RX1_P	91	I/O	2.5V	Bank 4A
55	HSMC1_TX1_N	80	I/O	2.5V	Bank 4A
56	HSMC1_RX1_N	93	I/O	2.5V	Bank 4A

57	+3.3V	-	Power	1A Max	Note 1
58	+12V	-	Power	1A Max	Note 2
59	HSMC1_TX2_P	82	I/O	2.5V	Bank 4A
60	HSMC1_RX2_P	95	I/O	2.5V	Bank 4A
61	HSMC1_TX2_N	84	I/O	2.5V	Bank 4A
62	HSMC1_RX2_N	97	I/O	2.5V	Bank 4A
63	+3.3V	-	Power	1A Max	Note 1
64	+12V	-	Power	1A Max	Note 2
65	HSMC1_TX3_P	86	I/O	2.5V	Bank 4A
66	HSMC1_RX3_P	105	I/O	2.5V	Bank 4A
67	HSMC1_TX3_N	88	I/O	2.5V	Bank 4A
68	HSMC1_RX3_N	107	I/O	2.5V	Bank 4A
69	+3.3V	-	Power	1A Max	Note 1
70	+12V	-	Power	1A Max	Note 2
71	HSMC1_TX4_P	94	I/O	2.5V	Bank 4A
72	HSMC1_RX4_P	109	I/O	2.5V	Bank 4A
73	HSMC1_TX4_N	96	I/O	2.5V	Bank 4A
74	HSMC1_RX4_N	111	I/O	2.5V	Bank 4A
75	+3.3V	-	Power	1A Max	Note 1
76	+12V	-	Power	1A Max	Note 2
77	HSMC1_TX5_P	98	I/O	2.5V	Bank 4A
78	HSMC1_RX5_P	113	I/O	2.5V	Bank 4A
79	HSMC1_TX5_N	100	I/O	2.5V	Bank 4A
80	HSMC1_RX5_N	115	I/O	2.5V	Bank 4A
81	+3.3V	-	Power	1A Max	Note 1
82	+12V	-	Power	1A Max	Note 2
83	HSMC1_TX6_P	102	I/O	2.5V	Bank 4A
84	HSMC1_RX6_P	121	I/O	2.5V	Bank 4A
85	HSMC1_TX6_N	104	I/O	2.5V	Bank 4A
86	HSMC1_RX6_N	123	I/O	2.5V	Bank 4A
87	+3.3V	-	Power	1A Max	Note 1
88	+12V	-	Power	1A Max	Note 2
89	HSMC1_TX7_P	110	I/O	2.5V	Bank 4A
90	HSMC1_RX7_P	133	I/O	2.5V	Bank 4A
91	HSMC1_TX7_N	112	I/O	2.5V	Bank 4A
92	HSMC1_RX7_N	135	I/O	2.5V	Bank 4A
93	+3.3V	-	Power	1A Max	Note 1
94	+12V	-	Power	1A Max	Note 2
95	HSMC1_CLKOUT1_P	114	O	2.5V	Bank 4A
96	HSMC1_CLKIN1_P	177	I	2.5V	Bank 8A
97	HSMC1_CLKOUT1_N	116	O	2.5V	Bank 4A
98	HSMC1_CLKIN1_N	179	I	2.5V	Bank 8A
99	+3.3V	-	Power	1A Max	Note 1
100	+12V	-	Power	1A Max	Note 2
101	HSMC1_TX8_P	118	I/O	2.5V	Bank 4A
102	HSMC1_RX8_P	137	I/O	2.5V	Bank 4A
103	HSMC1_TX8_N	120	I/O	2.5V	Bank 4A
104	HSMC1_RX8_N	139	I/O	2.5V	Bank 4A
105	+3.3V	-	Power	1A Max	Note 1
106	+12V	-	Power	1A Max	Note 2
107	HSMC1_TX9_P	122	I/O	2.5V	Bank 3B
108	HSMC1_RX9_P	141	I/O	2.5V	Bank 3B
109	HSMC1_TX9_N	124	I/O	2.5V	Bank 3B
110	HSMC1_RX9_N	143	I/O	2.5V	Bank 3B
111	+3.3V	-	Power	1A Max	Note 1
112	+12V	-	Power	1A Max	Note 2
113	HSMC1_TX10_P	138	I/O	2.5V	Bank 3B
114	HSMC1_RX10_P	145	I/O	2.5V	Bank 3B
115	HSMC1_TX10_N	140	I/O	2.5V	Bank 3B

116	HSMC1_RX10_N	147	I/O	2.5V	Bank 3B
117	+3.3V	-	Power	1A Max	Note 1
118	+12V	-	Power	1A Max	Note 2
119	HSMC1_TX11_P	142	I/O	2.5V	Bank 3B
120	HSMC1_RX11_P	149	I/O	2.5V	Bank 3B
121	HSMC1_TX11_N	144	I/O	2.5V	Bank 3B
122	HSMC1_RX11_N	151	I/O	2.5V	Bank 3B
123	+3.3V	-	Power	1A Max	Note 1
124	+12V	-	Power	1A Max	Note 2
125	HSMC1_TX12_P	146	I/O	2.5V	Bank 3B
126	HSMC1_RX12_P	155	I/O	2.5V	Bank 3B
127	HSMC1_TX12_N	148	I/O	2.5V	Bank 3B
128	HSMC1_RX12_N	157	I/O	2.5V	Bank 3B
129	+3.3V	-	Power	1A Max	Note 1
130	+12V	-	Power	1A Max	Note 2
131	HSMC1_TX13_P	150	I/O	2.5V	Bank 3B
132	HSMC1_RX13_P	159	I/O	2.5V	Bank 3B
133	HSMC1_TX13_N	152	I/O	2.5V	Bank 3B
134	HSMC1_RX13_N	161	I/O	2.5V	Bank 3B
135	+3.3V	-	Power	1A Max	Note 1
136	+12V	-	Power	1A Max	Note 2
137	HSMC1_TX14_P	154	I/O	2.5V	Bank 3B
138	HSMC1_RX14_P	163	I/O	2.5V	Bank 3B
139	HSMC1_TX14_N	156	I/O	2.5V	Bank 3B
140	HSMC1_RX14_N	165	I/O	2.5V	Bank 3B
141	+3.3V	-	Power	1A Max	Note 1
142	+12V	-	Power	1A Max	Note 2
143	HSMC1_TX15_P	164	I/O	2.5V	Bank 3B
144	HSMC1_RX15_P	167	I/O	2.5V	Bank 3B
145	HSMC1_TX15_N	166	I/O	2.5V	Bank 3B
146	HSMC1_RX15_N	169	I/O	2.5V	Bank 3B
147	+3.3V	-	Power	1A Max	Note 1
148	+12V	-	Power	1A Max	Note 2
149	HSMC1_TX16_P	168	I/O	2.5V	Bank 3B
150	HSMC1_RX16_P	171	I/O	2.5V	Bank 3B
151	HSMC1_TX16_N	170	I/O	2.5V	Bank 3B
152	HSMC1_RX16_N	173	I/O	2.5V	Bank 3B
153	+3.3V	-	Power	1A Max	Note 1
154	+12V	-	Power	1A Max	Note 2
155	HSMC1_CLKOUT2_P	178	O	2.5V	Bank 8A
156	HSMC1_CLKIN2_P	172	I	2.5V	Bank 8A
157	HSMC1_CLKOUT2_N	180	O	2.5V	Bank 8A
158	HSMC1_CLKIN2_N	174	I	2.5V	Bank 8A
159	+3.3V	-	Power	1A Max	Note 1
160	HSMC1_PRSNTN	85	O	2.5V	Bank 4A
161 - 172	GND	-	Power		

Notes:
1. The maximum total current supplied to external components from the +3.3V supply should be limited to less than 3.0A. The maximum current allowed per connector pin is 1A.
2. The maximum total current supplied to external components from the +12V supply should be limited to less than 2.0A. The maximum current allowed per connector pin is 1A.

Please see the following Intel documentation concerning the HSMC specification (https://www.intel.com/content/www/us/en/content-details/655196/high-speed-mezzanine-card-hsmc-specification.html).

Full HSMC JTAG Debug Interface – J302

Table 8 describes the pin-out of the Full HSMC JTAG interface on the MitySOM-5CSX development board. This allows for debug of JTAG supported HSMC cards/devices.

Table 8: J101 JTAG Pin Assignments

Pin	Schematic Signal	SoM Pin	Type	Standard	Notes
1	HSMC1_JTAG_TCK	-	-		J300 – Pin 35
2	GND	-	Power		
3	HSMC1_JTAG_TDO	-	-		J300 – Pin 37
4	+3.3V_EXT	-	Power	1A Max	Note 1
5	HSMC1_JTAG_TMS	-	-		J300 – Pin 36
6 – 8	RESERVED	-	-		
9	HSMC1_JTAG_TDI	-	-		J300 – Pin 38
10	GND	-	Power		

Partial HSMC Interface – J301

Table 9 describes the pin-out of the partial HSMC interface on the MitySOM-5CSX development board. The I/O "type" is in reference to the signal direction from the SoM/development board.

Table 9: J506 Connector Pin Assignments

Pin	Schematic Signal	J303 Pin	SoM Pin	Type	Standard	Notes
1 - 28	RESERVED	-	-	-		
29	HSMC2_GTX0_P	-	245	O		Transceiver
30	HSMC2_GRX0_P	-	238	I		Transceiver
31	HSMC2_GTX0_N	-	247	O		Transceiver
32	HSMC2_GRX0_N	-	240	I		Transceiver
33	HSMC2_SMSDA	-	58	I/O		Bank 4A
34	HSMC2_SMSCL	-	56	O		Bank 4A
35 – 40	RESERVED	-	-	-		
41	HSMC2_D1_P	-	65	I/O	2.5V	Bank 4A
42	HSMC2_D2_P	-	61	I/O	2.5V	Bank 4A
43	HSMC2_D1_N	-	67	I/O	2.5V	Bank 4A
44	HSMC2_D2_N	-	63	I/O	2.5V	Bank 4A
45	+3.3V	-	-	Power	1A Max	Note 1
46	+12V	-	-	Power	1A Max	Note 2
47	HSMC2_TX0_P	-	64	I/O	2.5V	Bank 4A
48	HSMC2_RX0_P	-	77	I/O	2.5V	Bank 4A
49	HSMC2_TX0_N	-	66	I/O	2.5V	Bank 4A
50	HSMC2_RX0_N	-	79	I/O	2.5V	Bank 4A
51	+3.3V	-	-	Power	1A Max	Note 1
52	+12V	-	-	Power	1A Max	Note 2
53	HSMC2_TX1_P	17	62/196	I/O	2.5V	Note 3
54	HSMC2_RX1_P	-	73	I/O	2.5V	Bank 4A
55	HSMC2_TX1_N	16	198	I/O	2.5V	Note 3
56	HSMC2_RX1_N	-	71	I/O	2.5V	Bank 4A
57	+3.3V	-	-	Power	1A Max	Note 1
58	+12V	-	-	Power	1A Max	Note 2
59	HSMC2_TX2_P	19	192	I/O	2.5V	Note 3
60	HSMC2_RX2_P	13	203	I/O	2.5V	Note 3
61	HSMC2_TX2_N	18	194	I/O	2.5V	Note 3
62	HSMC2_RX2_N	14	205	I/O	2.5V	Note 3
63	+3.3V	-	-	Power	1A Max	Note 1
64	+12V	-	-	Power	1A Max	Note 2
65	HSMC2_TX3_P	21	188	I/O	2.5V	Note 3
66	HSMC2_RX3_P	11	199	I/O	2.5V	Note 3
67	HSMC2_TX3_N	20	190	I/O	2.5V	Note 3
68	HSMC2_RX3_N	12	201	I/O	2.5V	Note 3
69	+3.3V	-	-	Power	1A Max	Note 1
70	+12V	-	-	Power	1A Max	Note 2
71	HSMC2_TX4_P	23	184	I/O	2.5V	Note 3
72	HSMC2_RX4_P	9	195	I/O	2.5V	Note 3
73	HSMC2_TX4_N	21	186	I/O	2.5V	Note 3
74	HSMC2_RX4_N	10	197	I/O	2.5V	Note 3
75	+3.3V	-	-	Power	1A Max	Note 1
76	+12V	-	-	Power	1A Max	Note 2
77	HSMC2_TX5_P	25	42	I/O	2.5V	Note 3
78	HSMC2_RX5_P	7	191	I/O	2.5V	Note 3
79	HSMC2_TX5_N	24	44	I/O	2.5V	Note 3
80	HSMC2_RX5_N	8	193	I/O	2.5V	Note 3
81	+3.3V	-	-	Power	1A Max	Note 1
82	+12V	-	-	Power	1A Max	Note 2

83	HSMC2_TX6_P	27	53	I/O	2.5V	Note 3
84	HSMC2_RX6_P	5	187	I/O	2.5V	Note 3
85	HSMC2_TX6_N	26	55	I/O	2.5V	Note 3
86	HSMC2_RX6_N	6	189	I/O	2.5V	Note 3
87	+3.3V	-	-	Power	1A Max	Note 1
88	+12V	-	-	Power	1A Max	Note 2
89	HSMC2_TX7_P	29	47	I/O	2.5V	Note 3
90	HSMC2_RX7_P	3	183	I/O	2.5V	Note 3
91	HSMC2_TX7_N	28	49	I/O	2.5V	Note 3
92	HSMC2_RX7_N	4	185	I/O	2.5V	Note 3
93	+3.3V	-	-	Power	1A Max	Note 1
94	+12V	-	-	Power	1A Max	Note 2
95 - 98	RESERVED	-	-	-		
99	+3.3V	-	-	Power	1A Max	Note 1
100	+12V	-	-	Power	1A Max	Note 2
101 - 104	RESERVED	-	-	-		
105	+3.3V	-	-	Power	1A Max	Note 1
106	+12V	-	-	Power	1A Max	Note 2
107 - 110	RESERVED	-	-	-		
111	+3.3V	-	-	Power	1A Max	Note 1
112	+12V	-	-	Power	1A Max	Note 2
113 - 116	RESERVED	-	-	-		
117	+3.3V	-	-	Power	1A Max	Note 1
118	+12V	-	-	Power	1A Max	Note 2
119 - 122	RESERVED	-	-	-		
123	+3.3V	-	-	Power	1A Max	Note 1
124	+12V	-	-	Power	1A Max	Note 2
125 - 128	RESERVED	-	-	-		
129	+3.3V	-	-	Power	1A Max	Note 1
130	+12V	-	-	Power	1A Max	Note 2
131 - 134	RESERVED	-	-	-		
135	+3.3V	-	-	Power	1A Max	Note 1
136	+12V	-	-	Power	1A Max	Note 2
137 - 140	RESERVED	-	-	-		
141	+3.3V	-	-	Power	1A Max	Note 1
142	+12V	-	-	Power	1A Max	Note 2
143 - 146	RESERVED	-	-	-		
147	+3.3V	-	-	Power	1A Max	Note 1
148	+12V	-	-	Power	1A Max	Note 2
149 - 152	RESERVED	-	-	-		
153	+3.3V	-	-	Power	1A Max	Note 1
154	+12V	-	-	Power	1A Max	Note 2
155	HSMC2_CLK_P	-	-	O		100MHz clock, U102, to HSMC device
156	RESERVED	-	-	-		
157	HSMC2_CLK_N	-	-	O		100MHz clock, U102, to HSMC device
158	RESERVED	-	-	-		
159	+3.3V	-	-	Power	1A Max	Note 1
160	HSMC2_PRSNTN	-	60	I		Bank 4A
161 - 172	GND	-	-	Power		

Notes:

1. The maximum total current supplied to external components from the +3.3V supply should be limited to less than 3.0A. The maximum current allowed per connector pin is 1A.
2. The maximum total current supplied to external components from the +12V supply should be limited to less than 2.0A. The maximum current allowed per connector pin is 1A.
3. These pins are only connected when using a module with expanded IO capabilities.

Please see the following Intel documentation concerning the HSMC specification (https://www.intel.com/content/www/us/en/content-details/655196/high-speed-mezzanine-card-hsmc-specification.html).

10/100/1000 Ethernet Interface – J500

The MitySOM-5CSX Development Kit provides a RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out as shown in Table 10 below. The Ethernet PHY, Micrel KSZ9031, will auto negotiate to the speed of the device it is connected to.

Table 10: J500 Ethernet RJ45 Pin Assignments

Pin	Signal	Type	Standard	Notes
1	TXRXA_P	I/O		
2	TXRXA_N	I/O		
3	TXRXB_P	I/O		
4	TXRXB_N	I/O		
5	TXRXC_P	I/O		
6	TXRXC_N	I/O		
7	TXRXD_P	I/O		
8	TXRXD_N	I/O		

Boot Configuration header – J106

The boot mode, as determined by the 10 CONFIG switches, is selected on the rising edge of the PWRONRSTn Reset Input Pin of the Cyclone V processor which is controlled by the PMIC of the MitySOM-5CSX module. Each boot configuration pin on the development kit is connected to a weak pull up, '1', unless a switch is closed which pulls that configuration pin down to ground, '0'.

The MitySOM-5CSX Development Kits default boot configuration mode is shown in Figure 3 below. As seen this equates to a boot configuration setting of S1 to S10, `0000011101`. Please reference the Cyclone V Technical Reference Manual for complete details on how the vast array of boot mode options.

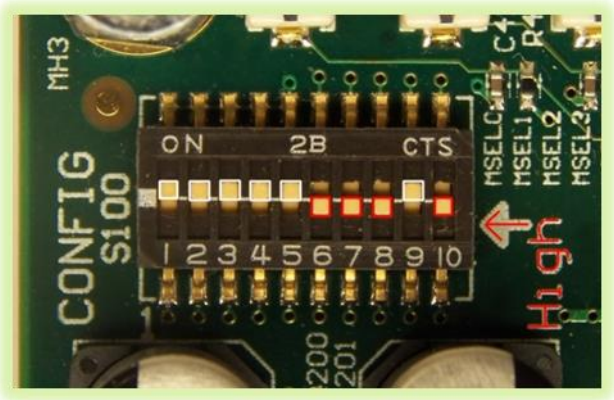


Figure 3: Default Development Kit Boot Jumper Mode

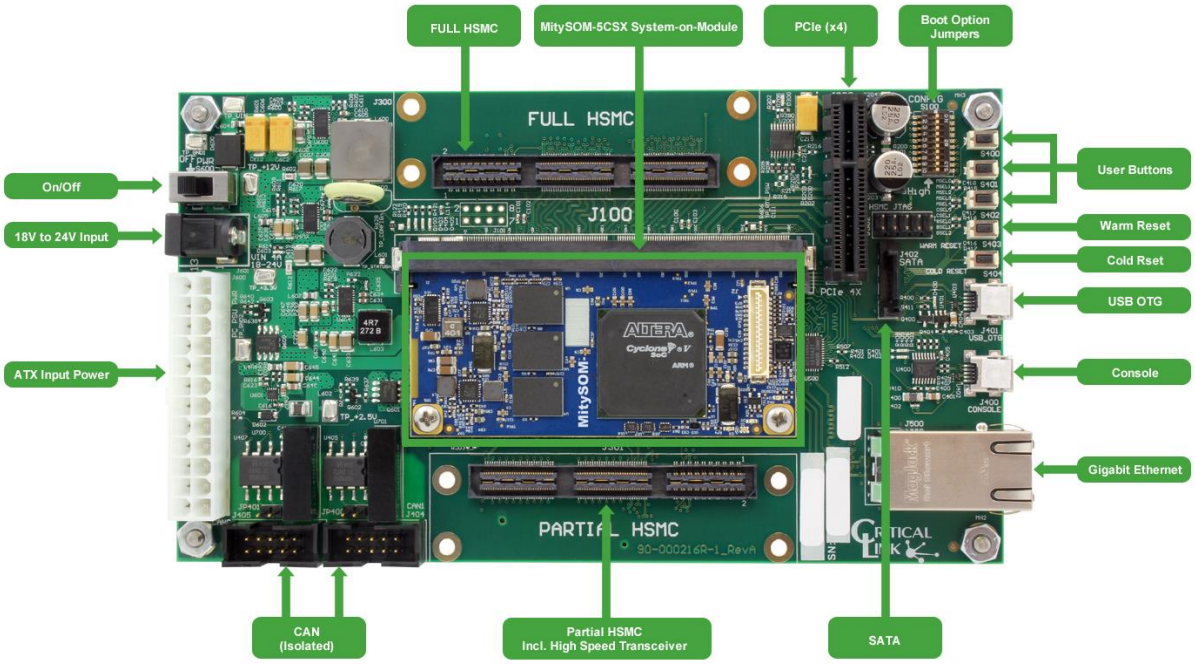
Included Components

The following table lists the components that are included with a MitySOM-5CSX Development Kit. See Table 12 for specific development kit ordering information.

Table 11: Included Items

Description	Interface Port	Qty. Included
MitySOM-5CSX Development Kit Board	n/a	Qty. 1
MitySOM-5CSX Module	J100	Qty. 1
Mini USB Cable for Debug Console	J400	Qty. 1
24V 2.7A AC to DC Supply	J601	Qty. 1
Ethernet cable – 7 foot	J500	Qty. 1
USB Drive with Development Environment	n/a	Qty. 1
Development Kit Schematic Files	n/a	
Development Kit Gerber Drawings	n/a	
Development Kit Bill Of Materials	n/a	
Development Kit Quick Start Guide	n/a	

MitySOM-5CSX Development Kit Board with MitySOM-5CSX Module



ORDERING INFORMATION

Development Kits

The following table lists the standard MitySOM-5CSX Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 12: Standard Model Numbers

Development Kit Model	Module Included	Module Junction Temp
80-000640	5CSX-H6-42A-RC	0ºC to 90º C
80-000639	5CSX-H6-42A-RI	-40ºC to 105º C
80-000708	5CSE-L2-3Y8-RC	0ºC to 90º C

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

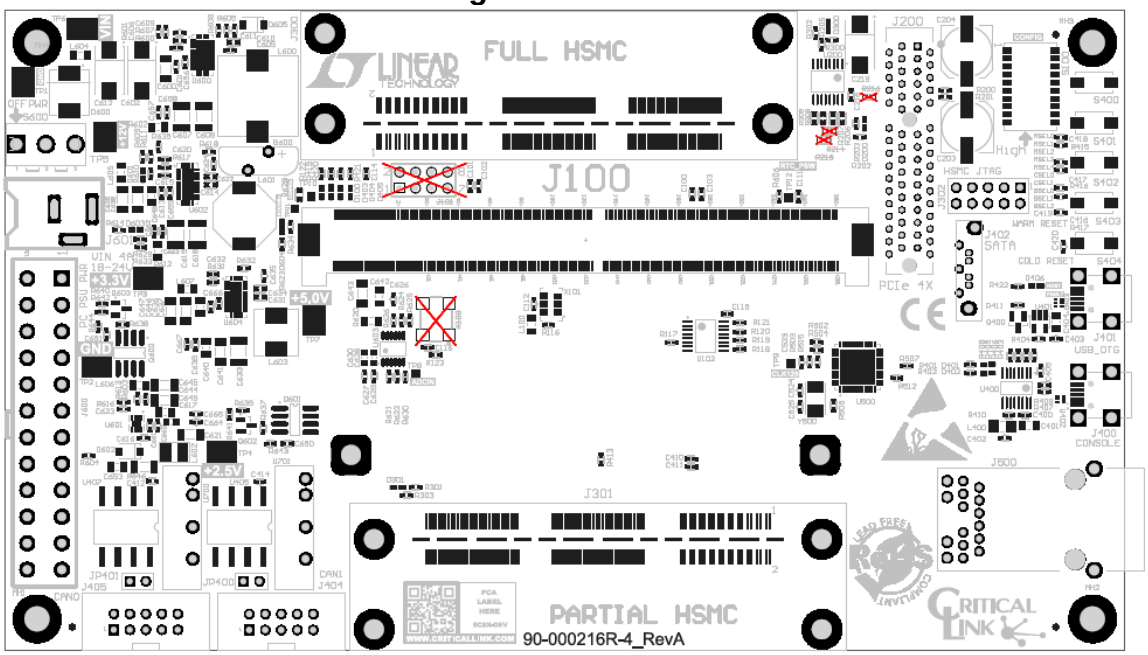


Figure 4: MitySOM-5CSX Development Kit Outline, Mounting Hole Locations, (Top View, inches)

REVISION HISTORY

Date	Change Description
12-JAN-2014	Initial revision.
31-APR-2014	Updates and changes from review and initial release.
6-AUG-2014	Updates and changes to encompass more detailed pin-out.
2-MAR-2023	Updated temperature range and standard model numbers.
27-NOV-2023	Updated RTC battery information, added components table on page 7 to clarify dev kit operating temp spec, updated HSMC spec url